In the Claims:

1. (Currently Amended) A variable-gain digital filter operating on input data and providing delayed input data including power control bits as a portion of said delayed input data and non-power control bits as another portion of said delayed input data, said digital filter having a construction in which a gain regulation circuit is incorporated inside the digital filter, said gain regulation circuit receiving said delayed input data and comprising: a first selector for selecting a first gain signal corresponding to said power control bits and a second gain signal corresponding to the non-power control bits ; and a first multiplier for directly multiplying some coefficient sequences with said first gain signal and other coefficient sequences with said second gain signal, said first and second gain signals output from said first selector.

2. (Currently Amended) A variable-gain digital filter according to claim 1 wherein:

said first multiplier of said gain regulation circuit multiplies the first and second gain signals that is outputted from said first selector with the coefficient sequences that are switched and outputted from a second selector for each fixed time interval;

an output of said first multiplier is multiplied at a second multiplier with ~~said~~ selected delayed input data, said selected delayed input data selected by a third selector that selects ones of said delayed input data from plural outputs of a shift register; and

an output of said second multiplier is then integrated by an integrator and outputted.

3. (Currently Amended) A variable-gain digital filter comprising:

a shift register that is constituted by a plurality of stages of flip-flops wherein each stage shifts input data and generates delayed data, a plurality of said delayed data corresponding to power control bits and ~~the remainder~~ a remainder of said delayed data not corresponding to power control bits;

a first selector for selecting a first gain signal and a second gain signal;

a second selector for selecting a coefficient sequence;

a third selector for selecting each delayed data~~delay output~~ of said shift register;

a first multiplier for multiplying said first gain signal with some outputs of said second selector resulting in a first product sequence, and for multiplying said second gain signal with other outputs of said second selector resulting in a second product sequence;

a second multiplier for multiplying outputs of said first multiplier containing said first product sequence with outputs of said third selector containing said plurality of said delayed data corresponding to said power control bits, and for multiplying other outputs of said first multiplier containing said second product sequence with other outputs of said third selector containing the remainder of said delayed data not corresponding to said power control ~~bit~~bits; and

an integrator for integrating an output of said second multiplier.

4. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity to form two circuits, each circuit having one of two first selectors, one of two second selectors, one of two third selectors, one of two first ~~multiplier~~ multipliers and one of two second multipliers, each of said two circuits handling one half of the delayed data; and

each of said two first, second and third selectors effects a selection ~~circuits switches output alternately~~ at each time interval of (T/n) × 2, where T is the duration of one time slot and n is a filter order.

5. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity to form two circuits, each circuit having one of two first selectors, one of two second selectors, one of two third selectors, one of two first ~~multiplier~~ multipliers and one of two second multipliers, each of said two circuits handling ~~a half divided load for each of said two first, two second and two third selectors and said two first and two second multipliers~~ half of the delayed data; and

each of said two first, second and third selectors effects a selection ~~circuits switches output alternately~~ at each time interval of T/n, where T is the duration of one time slot and n is a filter order.

6. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are increased in quantity m times to form m circuits, each circuit having one of m first selectors, one of m second ~~selectors~~ selectors, one of m third selectors, one of m first multipliers and one of m second multipliers, each of said m circuits handling only n/m delayed data allowing the processing speed of each of said m first multipliers and m second multipliers to be 1/m where m is an integer greater than one and n is a filter order.

7. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are increased in quantity m times to form m circuits, each circuit having one of m first selectors, one of m second ~~selectors~~ selectors, one of m third selectors, one of m first multipliers and one of m second multipliers, each of said m circuits handling only n/m delayed data to improve the processing speed of the variable-gain digital filter where m is an integer greater than one and n is a filter order.

8. (Currently Amended) A variable-gain digital filter comprising:

a shift register that is constituted by a plurality of stages of flip-flops wherein each stage shifts input data and generates delayed data ~~by each stage~~;

a first selector for selecting a gain;

a second selector for selecting a coefficient sequence;

a third selector for selecting each ~~delay output~~ delayed data of said shift register;

a first multiplier for multiplying an output of said first selector with an output of said second selector;

a second multiplier for multiplying an output of said first multiplier with an output of said third selector; and

an integrator for integrating an output of said second multiplier; and

wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity to form two circuits, each circuit having one of two first selectors, one of two second selectors, one of two third selectors, one of two first multiplier and one of two second multipliers, each of said two circuits handling ~~a half divided load for each of said two first, two second and two third selectors and said two first and two second multipliers~~ half of the delayed data; and

each of said two first, second and third selectors effects a selection ~~circuits switches output alternately~~ at each time interval of T/n, where T is the duration of one time slot and n is a filter order.

9. (Cancelled)

10. (Currently Amended) A variable-gain digital filter comprising:

a shift register that is constituted by a plurality of stages of flip-flops wherein each stage shifts input data and generates delayed data ~~by each stage~~;

a first selector for selecting a gain;

a second selector for selecting a coefficient sequence;

a third selector for selecting each ~~delay output~~ delayed data of said shift register;

a first multiplier for multiplying an output of said first selector with an output of said second selector;

a second multiplier for multiplying an output of said first multiplier with an output of said third selector; and

an integrator for integrating an output of at least said second multiplier; and

wherein:

said first, second, and third selectors and said first and second multipliers are increased in quantity m times to form m circuits, each circuit having one of m first selectors, one of m second ~~selectors~~ selectors, one of m third selectors, one of m first multipliers and one of m second multipliers, each of said m circuits handling only n/m delayed data allowing

the processing speed of each of said m first multipliers and m second multipliers to be 1/m where m is an integer greater than one and n is a filter order, said integrator integrating outputs of each of said m first multipliers and each of said second multipliers.

11. (Currently Amended) A variable-gain digital filter comprising:

a shift register that is constituted by a plurality of stages of flip-flops wherein each stage shifts input data and generates delayed data by each stage;

a first selector for selecting a gain;

a second selector for selecting a coefficient sequence;

a third selector for selecting each ~~delay output~~ delayed data of said shift register;

a first multiplier for multiplying an output of said first selector with an output of said second selector;

a second multiplier for multiplying an output of said first multiplier with an output of said third selector; and

an integrator for integrating an output of at least said second multiplier; and

wherein:

said first, second, and third selectors and said first and second multipliers are increased in quantity m times to form m circuits, each circuit having one of m first selectors, one of m second ~~selectors~~ selectors, one of m third selectors, one of m first multipliers and one of m second multipliers, each of said m circuits handling only n/m delayed data to improve the processing speed of the variable-gain digital filter where m is an integer greater than one and n is a filter order, said integrator integrating outputs of each of said m first multipliers and each of said second multipliers.